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2674	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/742,933	MIYACHI ET AL.	
	Examiner	Art Unit	
	William Boddie	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/23/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/23/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 12/23/03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 11,12,13,17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada et al. (US 6,219,017) in view of Nakanishi (US 5,488,389).

With respect to claim 1, Shimada discloses, a method for driving a group of pixels in a display device to display an image of a respective frame based on an interlace signal for displaying an image of a respective frame from video signals of a plurality of fields (figure 8), said method comprising the steps of:

(I) generating driving signals (Vn, Hn in fig. 13) based on video signals of a current field(In in fig. 13), so as to drive the group of pixels (10, in fig. 8) for displaying the frame image;

(II) modulating the driving signals for driving the group of pixels (7 in fig. 13), by referring to video signals of a previous field (8 in fig. 13);

in said step (II), the driving signals being respectively modulated for the group of pixels b referring to video signals of the previous field used to generate the driving signals for the respective pixels (col. 3, lines 59-63).

Shimada does not disclose expressly, (III) interpolating video signals for the previous field before modulating the driving signals, so as to generate video signals of

one frame; and (IV) interpolating video signals for the current field before modulating the driving signals, so as to generate video signals of one frame,

Nakanishi discloses (III) interpolating video signals for the previous field before modulating the driving signals, so as to generate video signals of one frame (fig. 28 and col. 17, 3rd paragraph); and

(IV) interpolating video signals for the current field before modulating the driving signals, so as to generate video signals of one frame (fig. 28 and col. 17, 3rd paragraph).

Shimada and Nakanishi are analogous art because they are from the same field of endeavor namely display device driving signal generation.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to utilize the multiple memory and line doubling, taught by Nakanishi, in the display modulation controls, taught by Shimada.

The motivation for doing so would have been to allow for the deinterlacing of the input video signal with greater speed.

Therefore it would have been obvious to combine Nakanishi with Shimada for the benefit of faster deinterlacing to obtain the invention as specified in claim 1.

With respect to claim 2, Shimada and Nakanishi disclose, the method as set forth in claim 1 (see above).

Shimada does not expressly disclose, wherein: in at least one of said step (III) and said step (IV), video signals are interpolated for a respective line of a field other than a target field of interpolation in such a manner that the interpolated video signals contain the same information as target field video signals of a frame line adjacent to the interpolated line.

Nakanishi discloses, wherein: in at least one of said step (III) and said step (IV), video signals are interpolated for a respective line of a field other than a target field of interpolation in such a manner that the interpolated video signals contain the same information as target field video signals of a frame line adjacent to the interpolated line (fig. 8).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to utilize the line doubling method, disclosed by Nakanishi, in Shimada's display modulation scheme.

The motivation for doing so would have been for it's easy implementation as an interpolation method.

Therefore it would have been obvious to combine Nakanishi with Shimada for the benefit of simplified circuitry to obtain the invention as specified in claim 2.

With respect to claim 11, no further limitations of claim 1 are found. Therefore, claim 11's rejection is based on the same grounds as shown above for the rejection of claim 1.

With respect to claim 12, Shimada and Nakanishi disclose, the driving device as set forth in claim 11 (see above), wherein the interlace signal produces an image of one frame from images of two fields (Nakanishi, col. 1, lines 46-48), wherein the current-field interpolating means includes a line memory (Nakanishi, 46 in fig. 38) for storing video signals of one line of the current field, and for outputting the video signals of one line twice by doubling a frequency of a dot clock (Nakanishi, 47 in fig. 38) for the interlace signal (Nakanishi, col. 25, lines 17-38), and wherein the previous-field interpolating means includes: a field memory (43 in fig. 44) for storing the video signals

of respective lines of the current field and holding the stored video signals until a next field; and control means (44 in fig. 44), by referring to the output of the line memory, for causing the field memory to store the video signals of respective lines of the current field, and for causing the field memory to output the video signals of respective lines of the previous field twice at the frequency of the line memory (Nakanishi, col. 25, lines 17-38).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to utilize the line doubling method, disclosed by Nakanishi, in Shimada's display modulation scheme.

The motivation for doing so would have been for its simplified circuitry as an interpolation method.

Therefore it would have been obvious to combine Nakanishi with Shimada for the benefit of simplified circuitry to obtain the invention as specified in claim 12.

With respect to claim 13, Shimada and Nakanishi disclose, the driving device as set forth in claim 11 (see above), wherein the interlace signal produces an image of one frame from images of two fields (Nakanishi, col. 1, lines 46-48), wherein the current-field interpolating means includes a current-field line memory (Nakanishi, 23 in fig. 25) for storing video signals of one line of the current field, and for outputting the video signals of one line twice by doubling a frequency of a dot clock for the interlace signal (c2 in fig. 26), and wherein the previous-field interpolating means includes a previous-field line memory (Nakanishi, 46 in fig. 44) for storing video signals of one line outputted from the field memory, and for outputting the stored video signals of one line twice at the frequency of the current-field line memory (Nakanishi, col. 25, lines 17-38).

While Nakanishi does not expressly disclose, wherein the current-and-previous video signal generating means includes a field memory for outputting the interlace signal with a delay of one field, Nakanishi does disclose similar embodiments (figs. 18, 44, and 49) which utilize field delay and field memories. With this in mind at the time of the invention, it would have been obvious to one of ordinary skill in the art to include a field memory in the current-and-previous field video signal generating means. The motivation for doing so would have been to allow corresponding pixel data to be used in the interpolation process.

Therefore it would have been obvious to combine the teachings of Nakanishi and Shimada for the benefit of corresponding pixel interpolation to obtain the invention as specified in claim 13.

With respect to claim 17, it would have been obvious to one of ordinary skill in the art to construct a computer program that would enable the implementation of the methods of claim 1. The motivation for doing so would be to make the aforementioned method viable as a piece of hardware in the commercial market. With regard to the recited steps of claim 17, as these steps do not further limit claim 1, they are rejected on the same merits as described above in claim 1.

With respect to claim 18, as it only further limits claim 17 by stating that the computer program is located on a recording medium, and further more as it is obvious to one of ordinary skill in the art to include a computer program on a recording medium, for portability reasons, claim 18 is rejected on the merits as claim 17.

3. Claims 3, 4, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada et al. (US 6,219,017) in view of Nakanishi (US 5,488,389) and further in view of Huang (US 6,295,091).

With respect to claim 3, Shimada and Nakanishi disclose, the method as set forth in claim 1 (see above), wherein two fields make up one frame (Nakanishi, col. 1, lines 46-48).

They do not expressly disclose, in as least one of said step (III) and said step (IV), video signals are interpolated for a respective line of a field other than a target field of interpolation in such a manner that the interpolated video signals contain the same information as video signals obtained by averaging target field video signals obtained by averaging target field video signals respectively of a pair of frame lines adjacent to the interpolated line.

Huang discloses, in as least one of said step (III) and said step (IV), video signals are interpolated for a respective line of a field other than a target field of interpolation in such a manner that the interpolated video signals contain the same information as video signals obtained by averaging target field video signals obtained by averaging target field video signals respectively of a pair of frame lines adjacent to the interpolated line (fig. 4).

Shimada and Nakanishi and Huang are all analogous art because they are from the same field of endeavor, namely methods and devices for deinterlacing video signals.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to utilize the adjacent line averaging method, taught by Huang, in Shimada/Nakanishi's display scheme.

The motivation for doing so would have been to eliminate motion artifacts that are present in other methods (Huang, col. 3, 50-53).

Therefore, it would have been obvious to combine Shimada, Nakanishi, and Huang for the benefit of eliminating motion artifacts to obtain the invention as specified in claim 3.

With respect to claim 4, Shimada and Nakanishi disclose, the method as set forth in claim 1 (see above), wherein: two fields make up one frame (see above);

They do not expressly disclose, and in at least one of said step (III) and said step (IV), video signals are interpolated for a respective line of a field other than a target field of interpolation in such a manner that the interpolated video signals contain the same information as target field video signals respectively of a pair of frame lines adjacent to the interpolated line, and that video signals for respective pixels of the interpolated line are generated based on video signals for a plurality of pixels in one of the pair of frame lines and based on video signals for a plurality of pixels in the other line of the pair of frame lines.

Huang discloses, in at least one of said step (III) and said step (IV), video signals are interpolated for a respective line of a field other than a target field of interpolation in such a manner that the interpolated video signals contain the same information as target field video signals respectively of a pair of frame lines adjacent to the interpolated line, and that video signals for respective pixels of the interpolated line are generated

based on video signals for a plurality of pixels in one of the pair of frame lines and based on video signals for a plurality of pixels in the other line of the pair of frame lines (fig. 6).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to utilize the interpolation method, taught by Huang, in Shimada/Nakanishi's display scheme.

The motivation for doing so would have been to eliminate "'jaggies' (stair-step artifacts on diagonal lines)" (Huang, col. 4, lines 20-22).

Therefore, it would have been obvious to combine Shimada, Nakanishi, and Huang for the benefit of eliminating stair-step artifacts to obtain the invention as specified in claim 4.

With respect to claim 5, Shimada and Nakanishi disclose, the method as set forth in claim 1 (see above), wherein: two fields make up one frame (see above);

They do not expressly disclose in at least one of said step (III) and said step (IV), video signals are interpolated in a respective line of a field other than a target field of interpolation based on target field video signals respectively of a pair of frame lines adjacent to the interpolated line and based on video signals in adjacent fields of the target field.

Huang discloses, they do not expressly disclose in at least one of said step (III) and said step (IV), video signals are interpolated in a respective line of a field other than a target field of interpolation based on target field video signals respectively of a pair of frame lines adjacent to the interpolated line and based on video signals in adjacent fields of the target field (fig. 5).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to utilize the interpolation method, taught by Huang, in Shimada/Nakanishi's display scheme.

The motivation for doing so would have been for a sharper picture than is present in other methods (Huang, col. 3, 53-56).

Therefore, it would have been obvious to combine Shimada, Nakanishi, and Huang for the benefit of a sharper picture to obtain the invention as specified in claim 5.

4. Claims 6, 7, 8, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada et al. (US 6,219,017) in view of Nakanishi (US 5,488,389) and further in view of Mizumaki (US 6,333,727).

With respect to claim 6, Shimada and Nakanishi disclose, the method as set forth in claim 1 (see above), wherein; two fields make up one frame (see above); and comparison between video signals of the current field and video signals of an earlier of previous two fields (Nakanishi, fig. 18).

They do not expressly disclose, the method further comprises the step of adjusting strength of modulation in said step (II) by referring to a result of comparison between video signals of the current field and video signals of an earlier of previous two fields.

Mizumaki discloses, the method further comprises the step of adjusting strength of modulation in said step (II) by referring to a result of comparison between video signals of the current field and video signals of an earlier of previous two fields (col. 8, lines 24-25).

Shimada and Nakanishi and Mizumaki are all analogous art because they are from the same field of endeavor, namely methods and devices for deinterlacing video signals.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to utilize the modulation adjustment teaching of Mizumaki, in Shimada/Nakanishi's display scheme.

The motivation for doing so would have been to lessen the occurrence of flicker in the displayed image. (Mizumaki, col. 3, lines 12-15).

Therefore, it would have been obvious to combine Shimada, Nakanishi, and Mizumaki for the benefit of better display quality to obtain the invention as specified in claim 6.

With respect to claim 7, Shimada and Nakanishi disclose, the method as set forth in claim 6 (see above).

They do not expressly disclose, said step of adjusting strength of modulation, modulation is stopped in said step (II) when the video signals of the current field substantially match the video signals of the earlier of the previous two fields.

Mizumaki discloses, said step of adjusting strength of modulation, modulation is stopped in said step (II) when the video signals of the current field substantially match the video signals of the earlier of the previous two fields (col. 8, lines 23-38).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to utilize the modulation adjustment teaching of Mizumaki, in Shimada/Nakanishi's display scheme.

The motivation for doing so would have been to lessen the occurrence of flicker in the displayed image. (Mizumaki, col. 3, lines 12-15).

Therefore, it would have been obvious to combine Shimada, Nakanishi, and Mizumaki for the benefit of better display quality to obtain the invention as specified in claim 7.

With respect to claim 8, Shimada and Nakanishi disclose, the method as set forth in claim 6 (see above), and video signals of the current field and the video signals of the earlier of the previous two fields (see above).

They do not expressly disclose, said step of adjusting strength of modulation, strength of modulation is gradually reduced from a full strength to zero strength according to a difference between the video signals of the current field and the video signals of the earlier of the previous two fields, if the difference falls within a predetermined range.

Mizumaki discloses, said step of adjusting strength of modulation, strength of modulation is gradually reduced from a full strength to zero strength according to a difference between the video signals of the current field and the video signals of the earlier of the previous two fields, if the difference falls within a predetermined range. (col. 8, lines 23-38).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to utilize the modulation adjustment teaching of Mizumaki, in Shimada/Nakanishi's display scheme.

The motivation for doing so would have been to lessen the occurrence of flicker in the displayed image. (Mizumaki, col. 3, lines 12-15).

Therefore, it would have been obvious to combine Shimada, Nakanishi, and Mizumaki for the benefit of better display quality to obtain the invention as specified in claim 8.

With respect to claim 15, Shimada and Nakanishi disclose, the driving device as set forth in claim 11(see above), wherein the interlace signal produces an image of one frame from images of two fields (Nakanishi, col. 1, lines 46-48).

The following portions of claim 15 are simply recitation of the limitations of claim 13: wherein the current-field interpolating means includes a current-field line memory for storing video signals of one line of the current field, and for outputting the stored video signals of one line twice by doubling a frequency of a dot clock for the interlace signal, and wherein the previous-field interpolating means includes a previous-field line memory for storing the video signals of one line outputted from the field memory, and for outputting the stored video signals of one line twice at the frequency of the current-field line memory. Therefore these limitations are rejected on the same merits as shown above in claim 13.

Nakanishi further discloses, and said driving device further comprises: a field memory (3,4 in fig. 18) for storing the video signals of the current field until input of one of a later of next two fields; control means for video signals causing the field memory to output video signals of one line of the previous field alternately with video signals of one line of a previous-corresponding-field at the frequency of the current-field line memory (5 in fig. 18, and Nakanishi, col. 25, lines 17-38); and a field line memory for storing the video signals of one line of the previous-corresponding-field outputted from the field

memory, and for outputting the stored video signals of one line of the previous-corresponding-field twice at the frequency of the current-field line memory (fig. 44).

While Nakanishi does not expressly disclose multiple field memories in the same circuitry with multiple line memories, Nakanishi does individually disclose both (fig. 18 and fig. 38). Nakanishi also later discloses a field memory coupled to a line memory (fig. 44 and fig. 49). It would have been obvious to one of ordinary skill in the art, at the time of the invention, to combine these teachings of Nakanishi and couple multiple field memories with multiple line memories. The motivation for doing so would have been to allow further control over the signals, which are being used for interpolation in order to arrive at a higher quality driving signal.

Shimada and Nakanishi do not disclose, wherein the driving signal generating means includes: comparing means for comparing the video signals of the current field outputted from the current-field interpolating means with the video signals of the previous-corresponding-field with respect to each pixel, and for outputting a result of comparison for each pixel; and adjusting means for adjusting, based on the result of comparison, strength of modulation for the driving signals of the respective pixels.

Mizumaki discloses, the further limitations of claim 6.

The following portions of claim 15 are simply recitation of the limitations of claim 6: and wherein the driving signal generating means includes: comparing means for comparing the video signals of the current field outputted from the current-field interpolating means with the video signals of the previous-corresponding-field with respect to each pixel, and for outputting a result of comparison for each pixel; and adjusting means for adjusting, based on the result of comparison, strength of

modulation for the driving signals of the respective pixels. Therefore these limitations are rejected on the same merits as shown above in claim 6.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine these teachings of Shimada, Nakanishi, and Mizumaki for the benefit of achieving a more efficient driving signal upon output to obtain the invention as specified in claim 15.

With respect to claim 16, Shimada and Nakanishi disclose, the driving device as set forth in claim 11 (see above).

The following portions are merely recitation of claim 15: wherein the interlace signal produces an image of one frame from images of two fields, and wherein the current-field interpolating means includes a current-field line memory for storing video signals of one line of the current field, and for outputting the stored video data of one line twice by doubling a frequency a dot clock for the interlace signal, and said driving device further comprises: a field memory for storing the video signals of the current field until input of a later of next two fields; and control means for causing the field memory to output the video signals of one line of the previous field alternately with video signals of one line of a previous-corresponding-field at the frequency of the current-field line memory, and wherein the previous-field interpolating means includes a previous-field line memory for storing the video signals of one line outputted from the field memory, and for outputting the stored video signals of one line twice at the frequency of the current-field line memory, and wherein the driving signal generating means includes: comparing means for comparing, with respect to each pixel, the video signals of the previous-corresponding-field with every other lines of the video signals outputted from

the current-field interpolating means, and for outputting a result of comparison for each pixel; and adjusting means for adjusting, based on the pixel-wise output of the comparison-result line memory, strength of modulation for the driving signals of the respective pixels.

Therefore the above portions are rejected on the same basis as stated above in claim 15.

The only further limiting factor of claim 16 is: A comparison-result line memory for storing the result of comparison for one line, and for outputting the stored result twice at the frequency of the current-field line memory.

Mizumaki discloses the use of memories in the comparison and gray-scale calculations (elements 3 and 4 in fig. 1).

Nakanishi discloses current-field line memories that output data at twice the speed (see above).

At the time of the invention it would have been obvious to one of ordinary skill in the art to couple a line memory to the comparison-result.

The motivation for doing so would have been to use this result in conjunction with other data, and the driving signals would result in better quality if previous comparison data were used to alter the current video signals.

Therefore it would have been obvious to combine Mizumaki, Nakanishi, and Shimada for the benefit of better driving signals to obtain the invention as specified in claim 16.

5. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada et al. (US 6,219,017) in view of Nakanishi (US 5,488,389) and further in view of Gadeyne et al. (US 6,909,472).

With respect to claim 9, Shimada and Nakanishi disclose, the method as set forth in claim 1 (see above).

They do not expressly disclose, in said step (II), the driving signals for the group of pixels are modulated so as to facilitate a grayscale level transition from the previous field to the current field; and the grayscale level transition in said step (II) is facilitated to such an extent that, when a pixel undergoes a grayscale level transition from the previous field to the current field by repeating a cycle of grayscale level transition between a first grayscale level and a second grayscale level, an integrated value of luminance for the pixel takes an intermediate value between the first grayscale level and the second grayscale level by causing whichever faster of a response speed with the strongest level of facilitation for a first-to-second grayscale level transition and a response speed with the strongest level of facilitation for a second-to-first grayscale level transition to approach whichever slower of the two response speeds.

Gadeyne discloses, in said step (II), the driving signals for the group of pixels are modulated so as to facilitate a grayscale level transition from the previous field to the current field; and the grayscale level transition in said step (II) is facilitated to such an extent that, when a pixel undergoes a grayscale level transition from the previous field to the current field by repeating a cycle of grayscale level transition between a first grayscale level and a second grayscale level, an integrated value of luminance for the pixel takes an intermediate value between the first grayscale level and the second

grayscale level by causing whichever faster of a response speed with the strongest level of facilitation for a first-to-second grayscale level transition and a response speed with the strongest level of facilitation for a second-to-first grayscale level transition to approach whichever slower of the two response speeds (col. 3, lines 45-52).

Shimada and Nakanishi and Gadeyne are all analogous art because they are from the same field of endeavor, namely generation of driving signals to be applied to displays.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the gradiation response embodiment of Gadeyne, with the display circuitry disclosed by Shimada and Nakanishi.

The motivation for doing so would have been to eliminate motion artifacts caused by different luminance response times (Gadeyne, abstract).

Therefore, it would have been obvious to combine Shimada and Nakanishi and Gadeyne for the benefit of eliminating motion artifacts to obtain the invention as specified in claim 9.

With respect to claim 10, Shimada, Nakanishi, and Gadeyne disclose, the method as set forth in claim 9 (see above).

Shimada and Nakanishi do not expressly disclose, the grayscale level transition in said step (II) is facilitated in such a manner that a grayscale level transition with the slowest response speed with the strongest facilitation determines response speeds of other grayscale level transitions, with the slowest response speed substantially matching the other response speeds.

Gadeyne discloses, the grayscale level transition in said step (II) is facilitated in such a manner that a grayscale level transition with the slowest response speed with the strongest facilitation determines response speeds of other grayscale level transitions, with the slowest response speed substantially matching the other response speeds (col. 3, lines 45-52).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the gradiation response embodiment of Gadeyne, with the display circuitry disclosed by Shimada and Nakanishi.

The motivation for doing so would have been to eliminate motion artifacts caused by different luminance response times (Gadeyne, abstract).

Therefore, it would have been obvious to combine Shimada and Nakanishi and Gadeyne for the benefit of eliminating motion artifacts to obtain the invention as specified in claim 10.

6. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada et al. (US 6,219,017) in view of Nakanishi (US 5,488,389) and further in view of Choquet et al. (US 4,937,667).

With respect to claim 14, Shimada and Nakanishi disclose, the driving device as set forth in claim 11 (see above),

They do not expressly disclose, further comprising: corresponding-field video signal generating means for storing the video signals of the current field until input of a field having video signals on corresponding positions, and for outputting the stored video signals as corresponding-field video signals, wherein the driving signal generating means compares the corresponding-field video signals with the video signals of the

current field, and, based on a result of comparison, varies strength of facilitation of a grayscale level transition from the previous to current field, so as to generate the driving signals.

Choquet discloses, further comprising: corresponding-field video signal generating means for storing the video signals of the current field until input of a field having video signals on corresponding positions (MT and ML in fig. 2, also col. 2, lines 63, 66), and for outputting the stored video signals as corresponding-field video signals, wherein the driving signal generating means compares (CG in fig. 2) the corresponding-field video signals (ML(t-1) in fig. 5) with the video signals of the current field (ML(t-1) in fig. 5), and, based on a result of comparison, varies strength of facilitation of a grayscale level transition (CPG in fig. 2) from the previous to current field, so as to generate the driving signals.

Shimada, Nakanishi and Choquet are all analogous art because they are from the same field of endeavor processing interlaced video signals.

At the time of the invention it would have been obvious to one of ordinary skill in the art to combine the gradiant calculation methods of Choquet with the display circuitry of Shimada and Nakanishi.

The motivation for doing so would have been to deinterlace video signals more simply, faster, and more effectively (Choquet, col. 2, line 16).

Therefore it would have been obvious to combine Shimada, Nakanishi and Choquet for the benefit of more effective deinterlacing to obtain the invention as specified in claim 14.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Arimoto et al. (US 2003/0090449) concerns line memory output speeds. Otera (US 6,507,346) discloses a means of pixel interpolation. Iwaki (US 6,567,097) also concerns data interpolation in interlaced fields. Finally, Wang et al. (Re. 35,093) deals with systems for coding even fields of interlaced video signals.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Will Boddie whose telephone number is (571) 272-0666. The examiner can normally be reached on Monday through Friday, 8:00 - 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Edouard can be reached on (571) 272-7603. Please note the new Central Fax Number 571-273-8300. Faxes sent to the old number, 703-872-9306, will be routed to the new number until September 15, 2005.

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Wlb
7/27/05

REGINA LIANG
PRIMARY EXAMINER